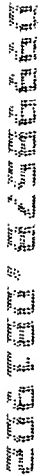


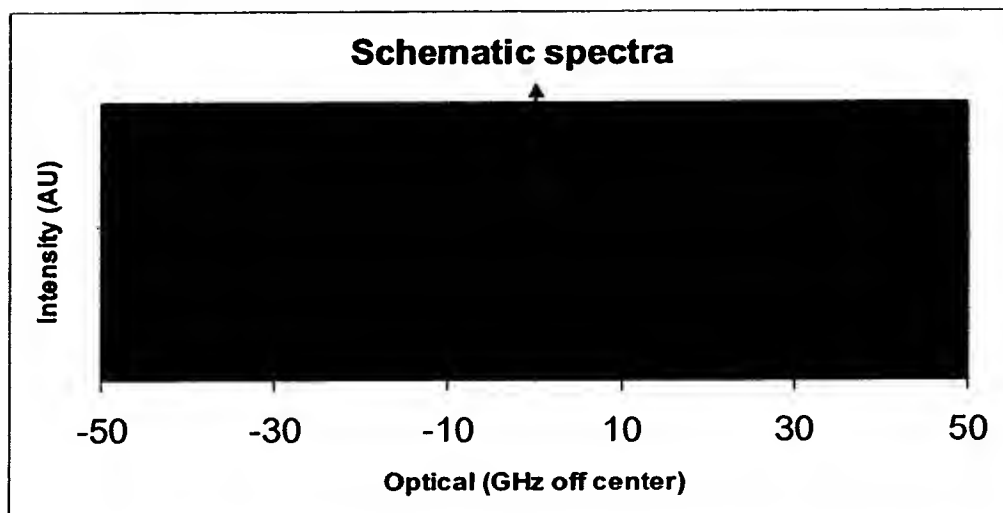
17



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FIG. 2

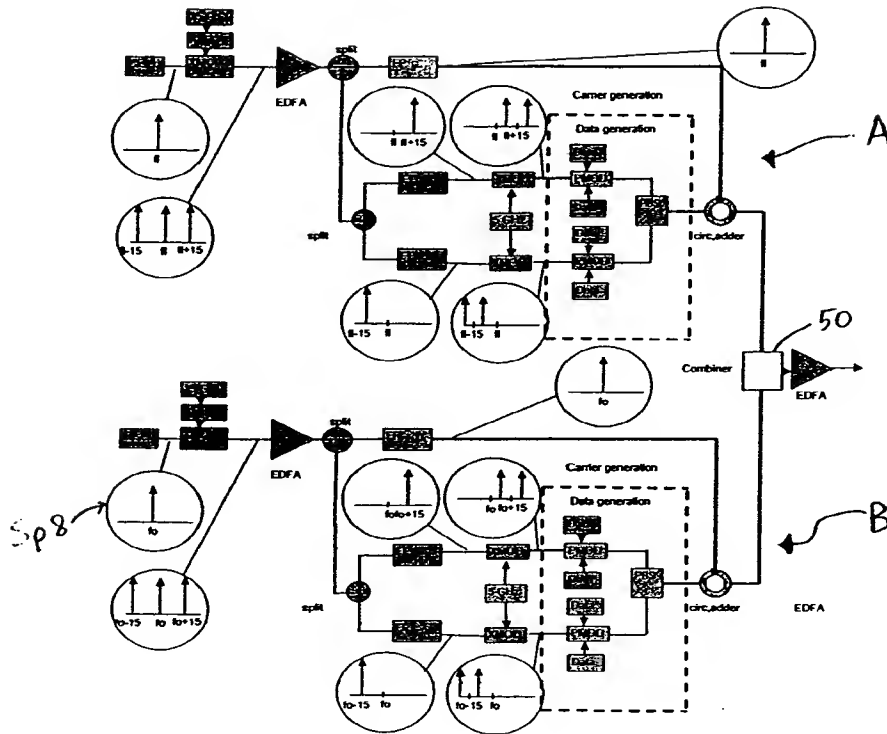


2006780/B/2556651



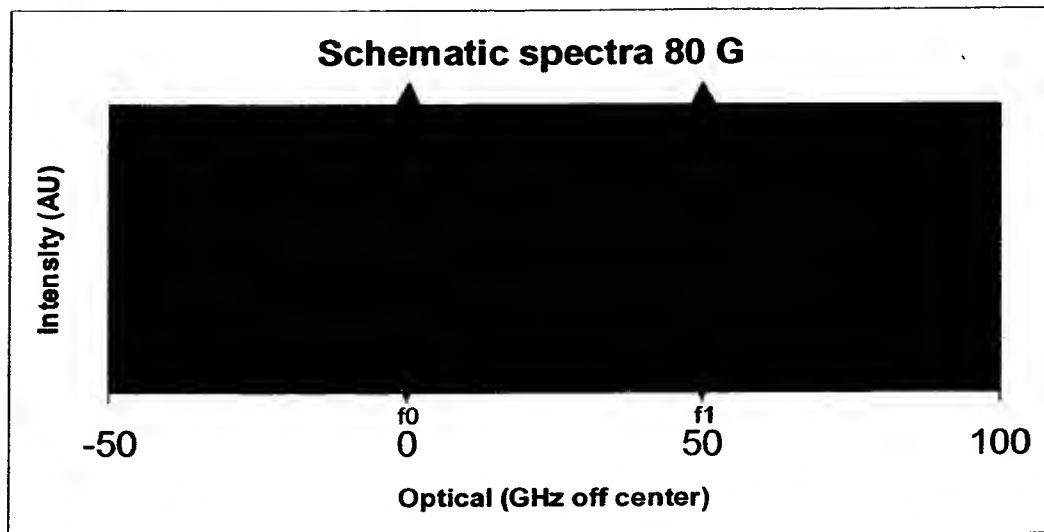
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FIG. 3



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FIG. 4



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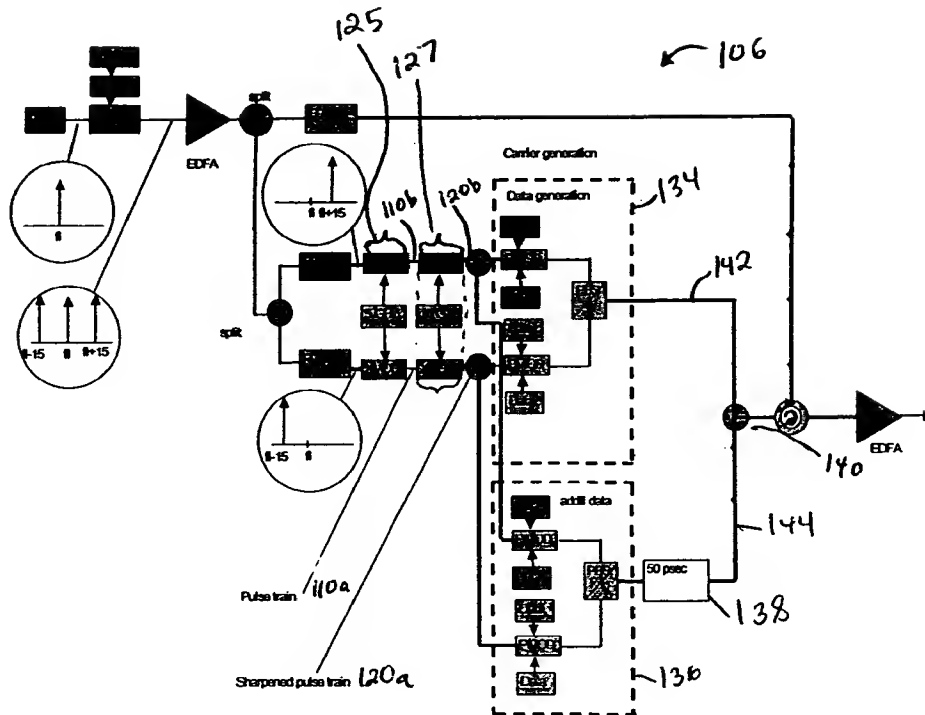
A circular stamp from the Office of Intellectual Property (OIPE). The text "OIPE" is at the top, "JC102" is at the top right, "AUG 19 2002" is in the center, and "PATENT & TRADEMARK OFFICE" is at the bottom.





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FIG. 6



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Fig. 7A

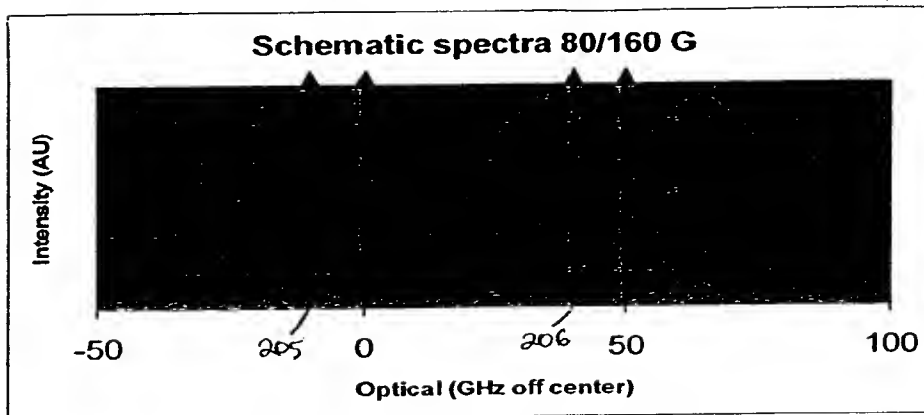


Fig. 7B

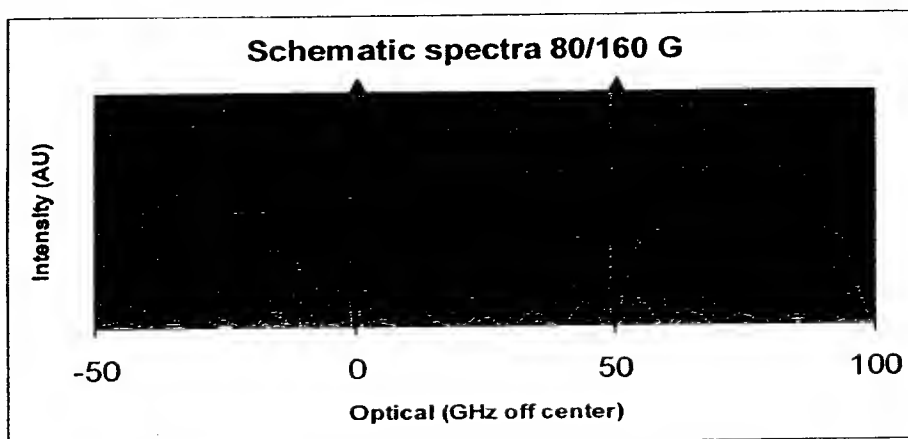
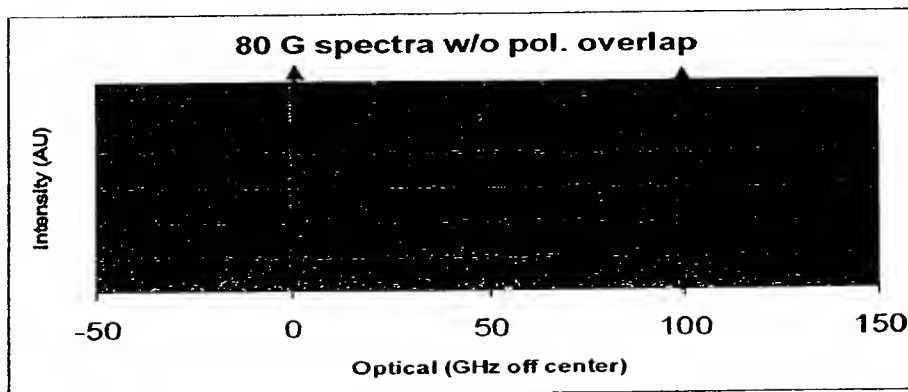


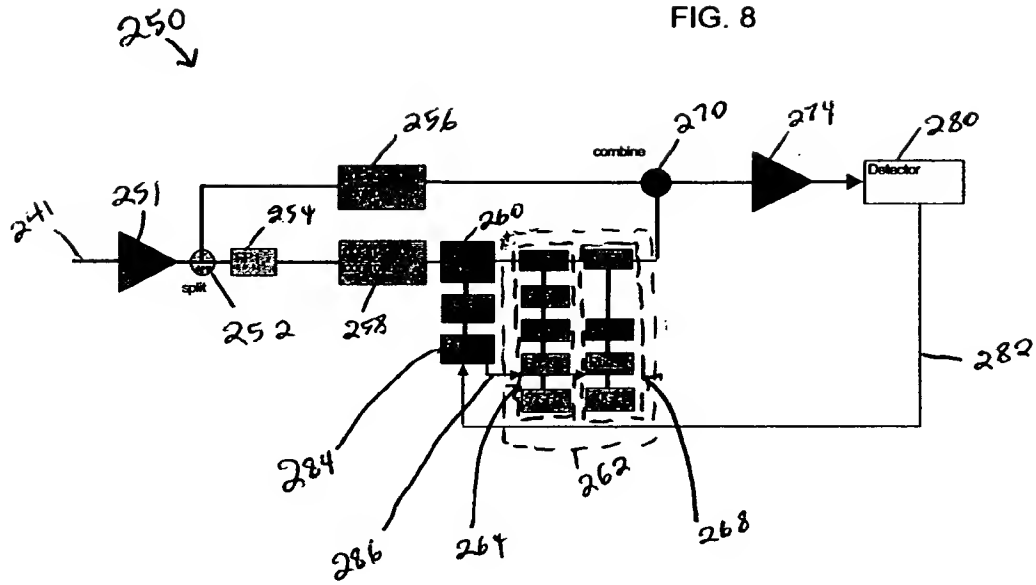
Fig. 7C



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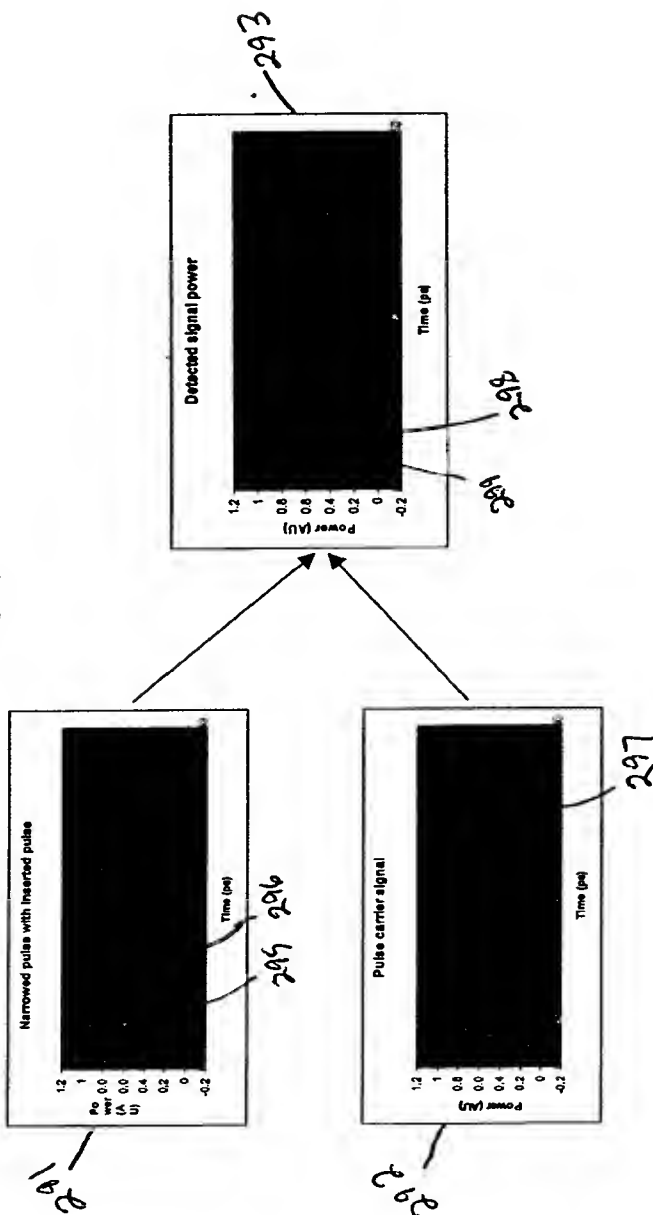
FIG. 8



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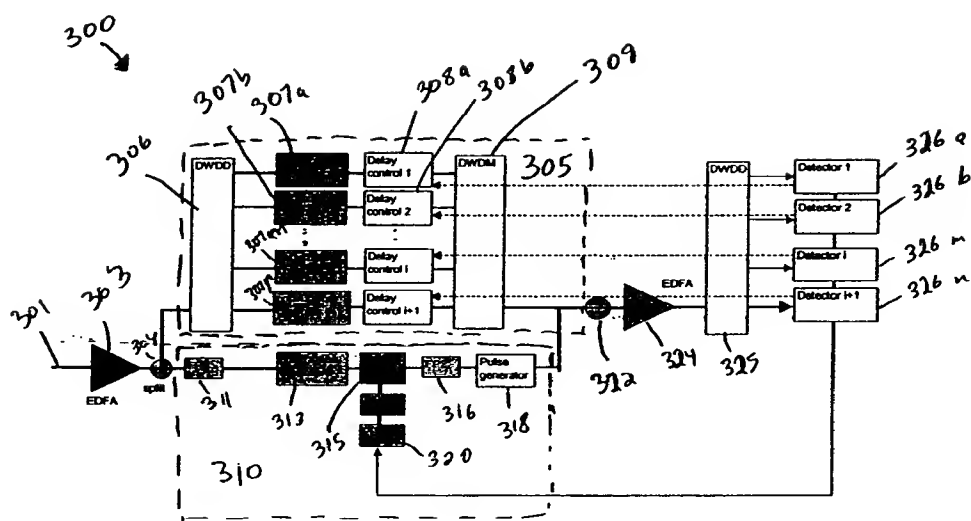
FIG. 9



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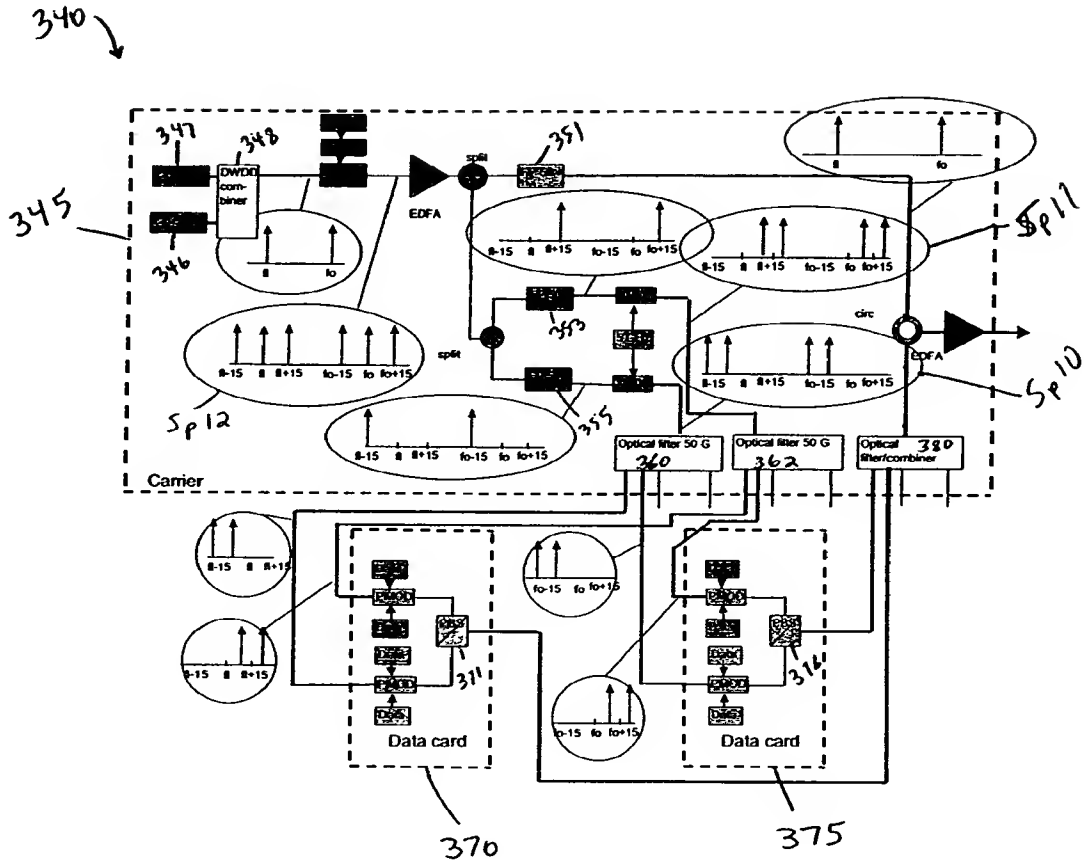
FIG. 10



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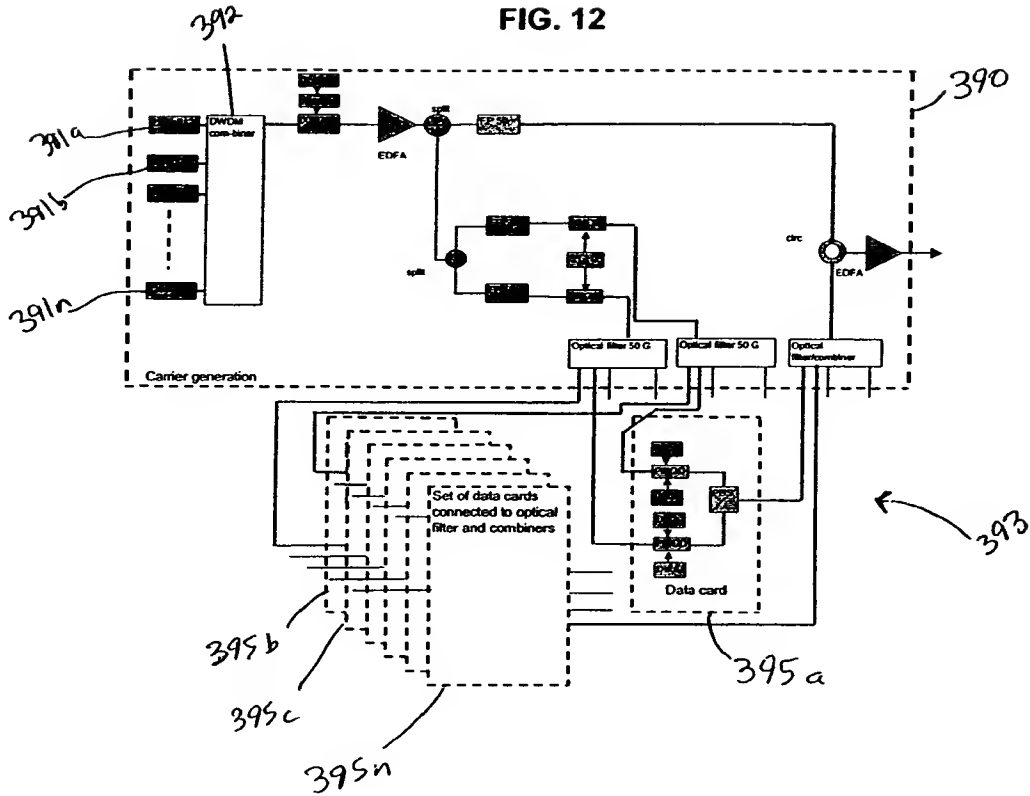
FIG. 11



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FIG. 12



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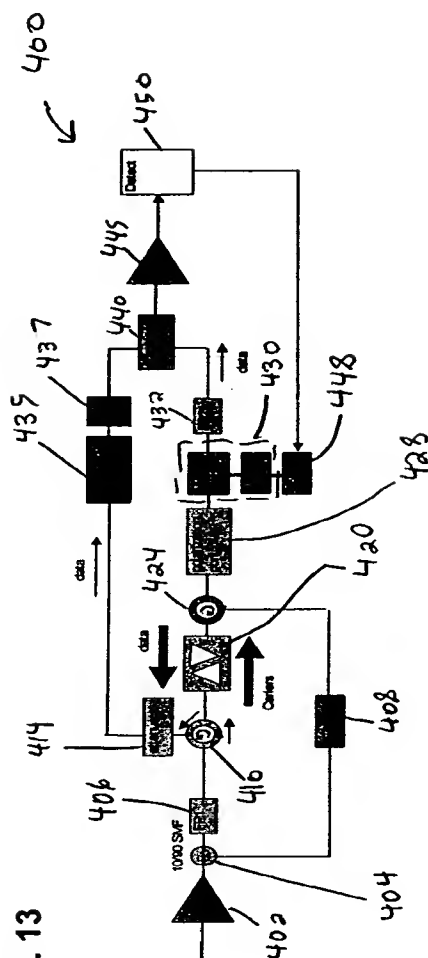




FIG. 14A

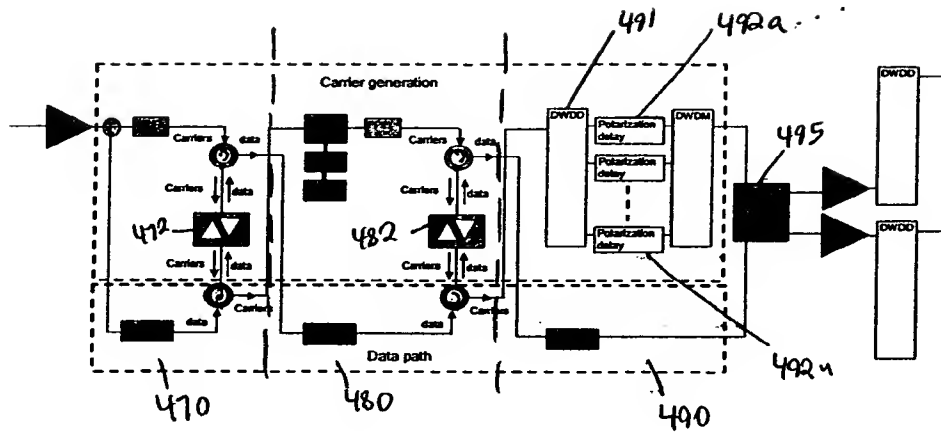
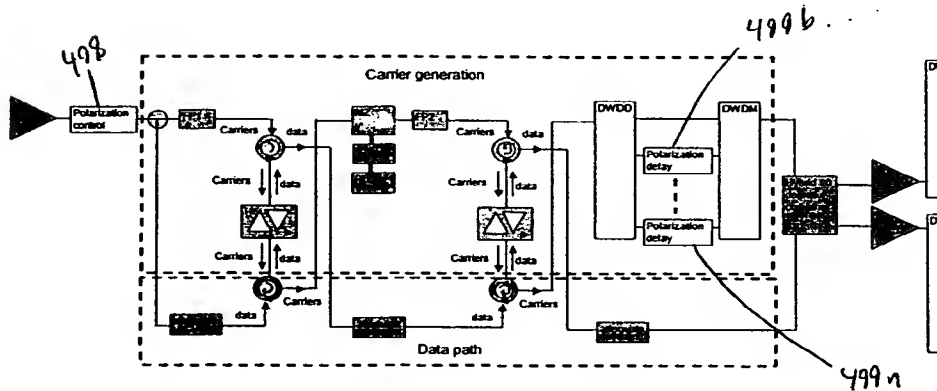


FIG. 14B



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FIG. 15

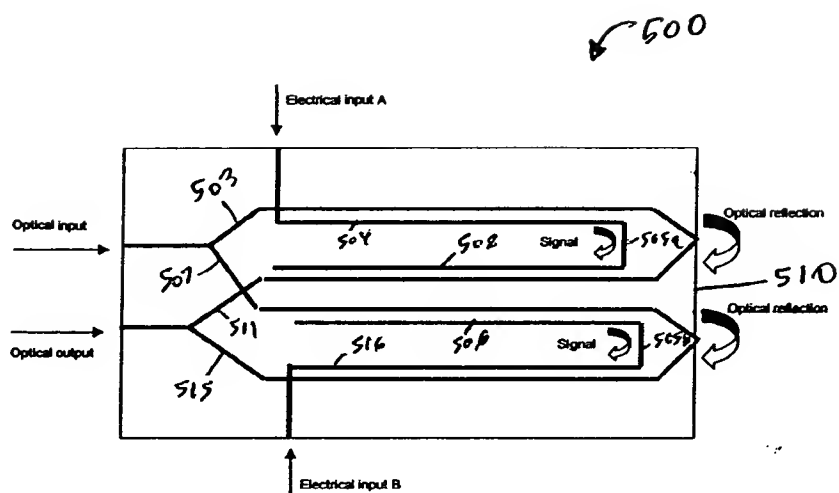
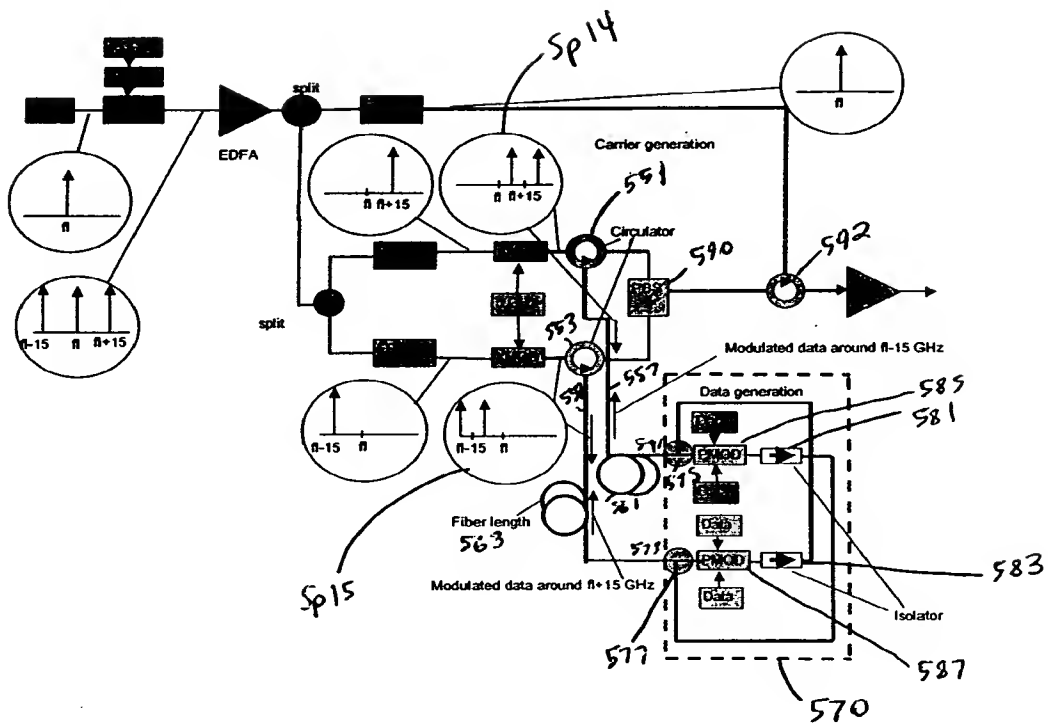


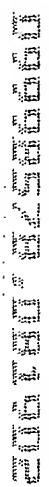


FIG. 16



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Figure 1 is a block diagram of a system for generating a modulated carrier. The diagram shows a signal flow starting from a data source (Sp16) through an EDFA amplifier, then through a series of mixers and filters (601, 603, 604, 605, 607, 608, 609, 611, 613, 615, 655) to produce a 'Modulated data around f+15 GHz' signal. A 'Reverse modulated carrier' (650) is also shown, which is a signal around f-15 GHz. The system includes a 'Data generation card' (620) with components like S1, S2, F1, F2, L1, L2, M1, M2, and O2. The diagram is heavily annotated with handwritten labels and numbers.



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FIG. 18A

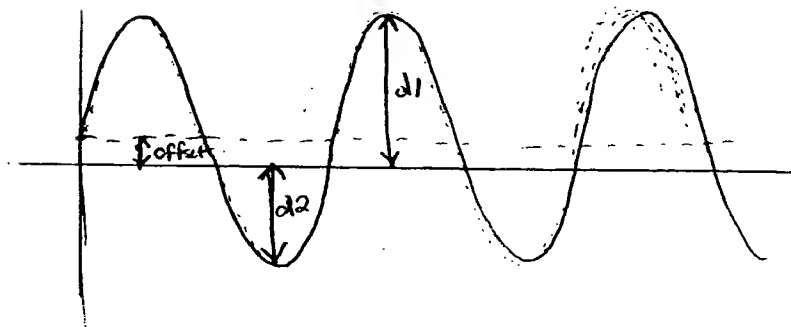
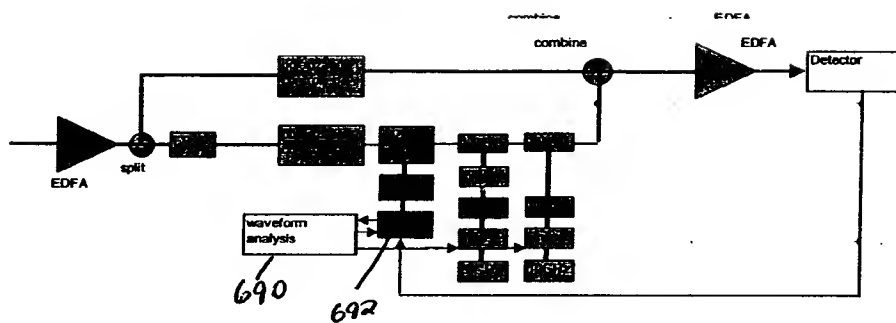


FIG. 18B



FIG. 19

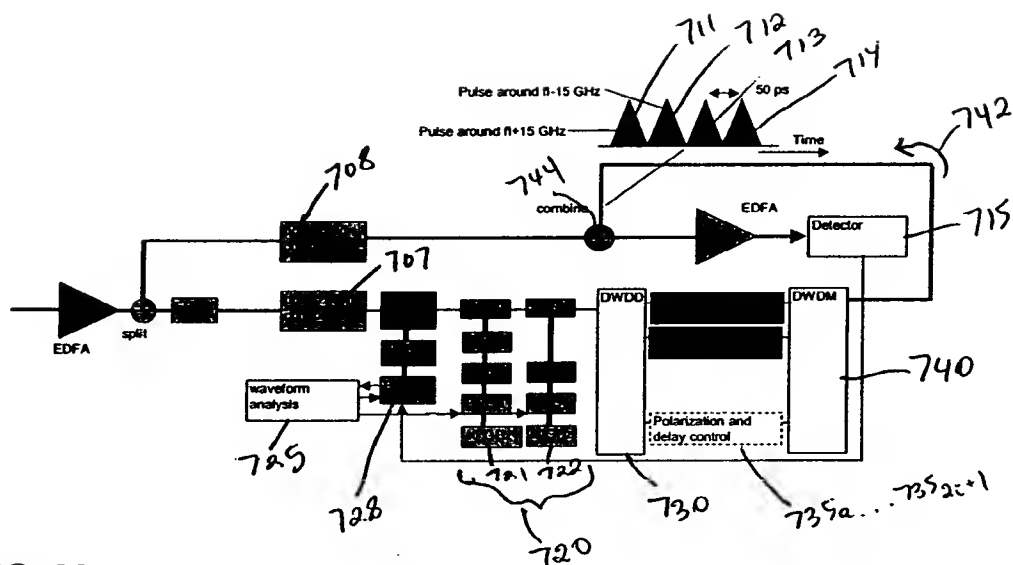
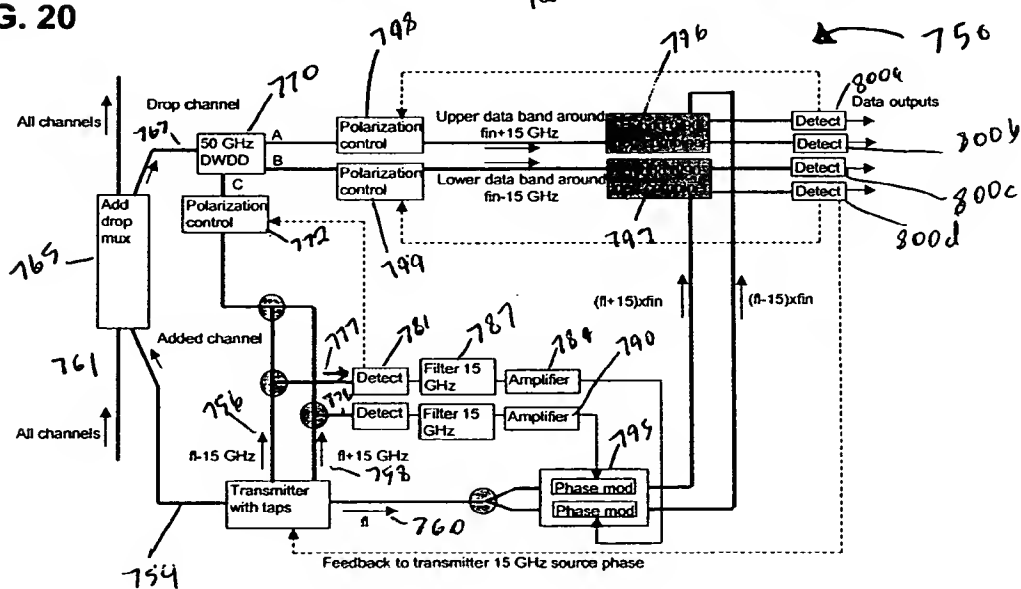


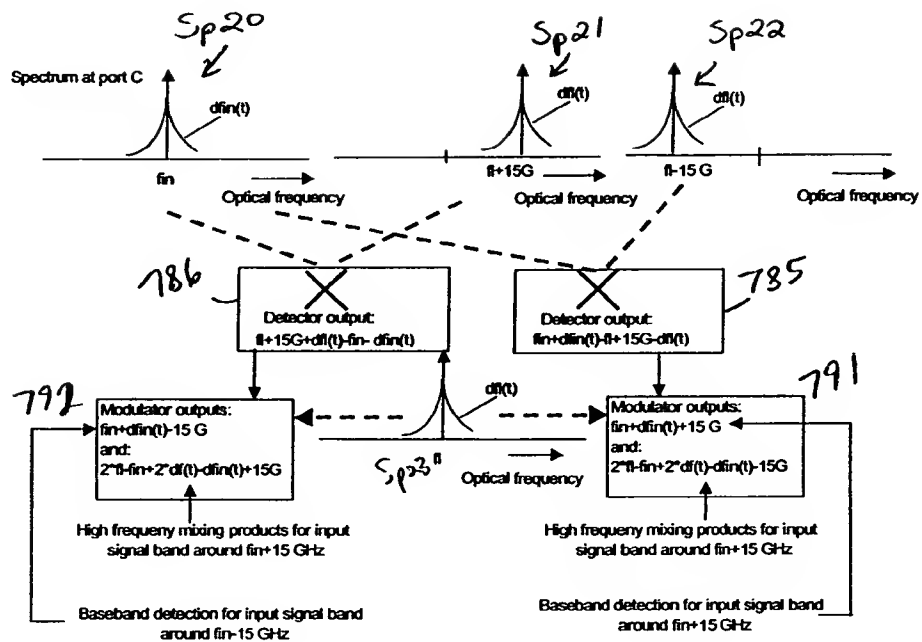
FIG. 20





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FIG. 21





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FIG. 22

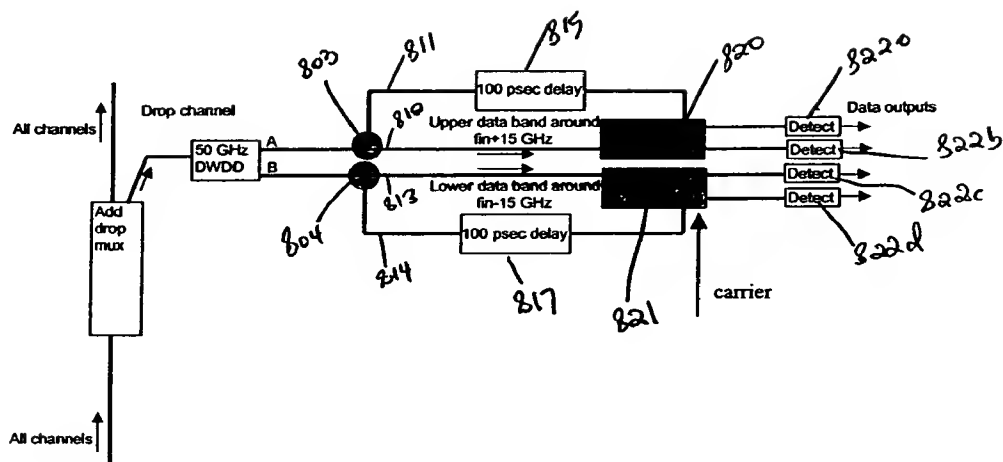
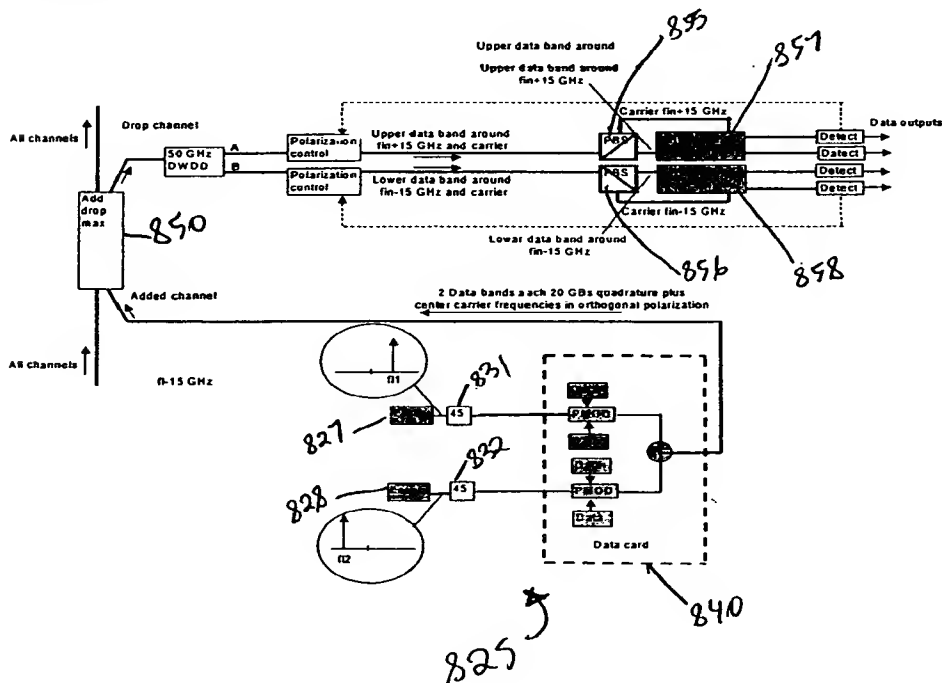
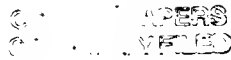
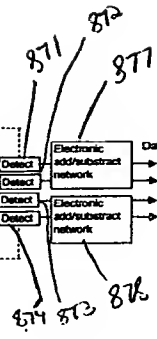
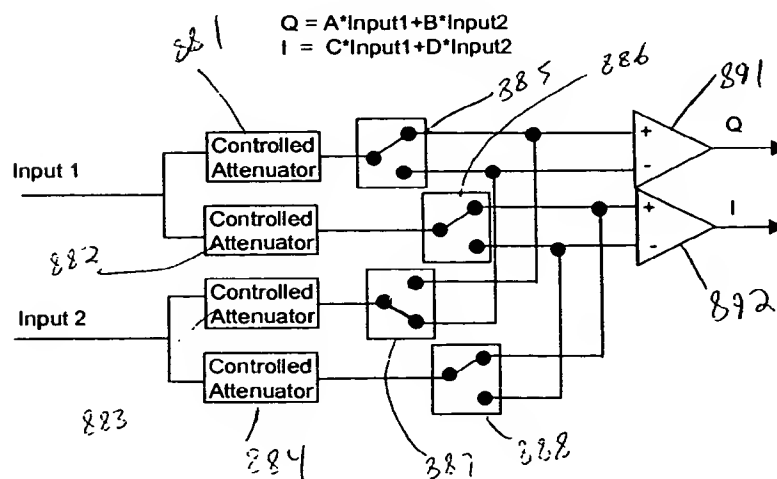


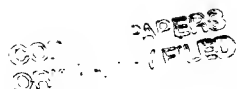
FIG. 23



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[illegible]

[illegible]
$$\begin{aligned} Q &= A \cdot \text{Input1} + B \cdot \text{Input2} \\ I &= C \cdot \text{Input1} + D \cdot \text{Input2} \end{aligned}$$




900

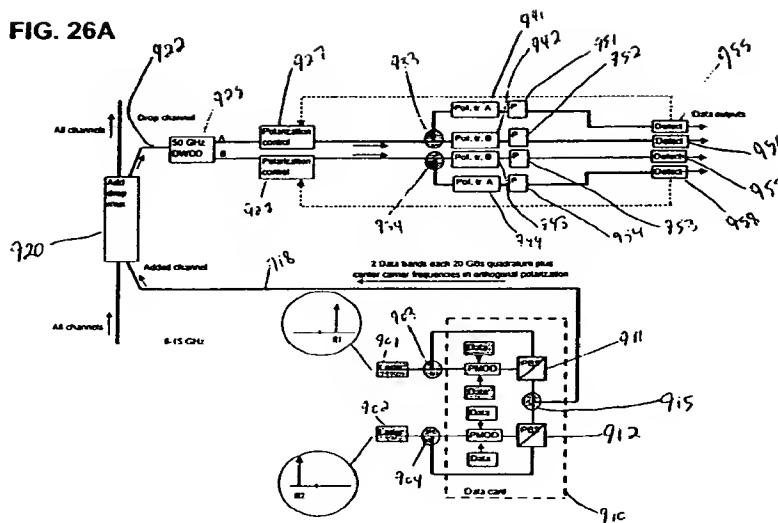
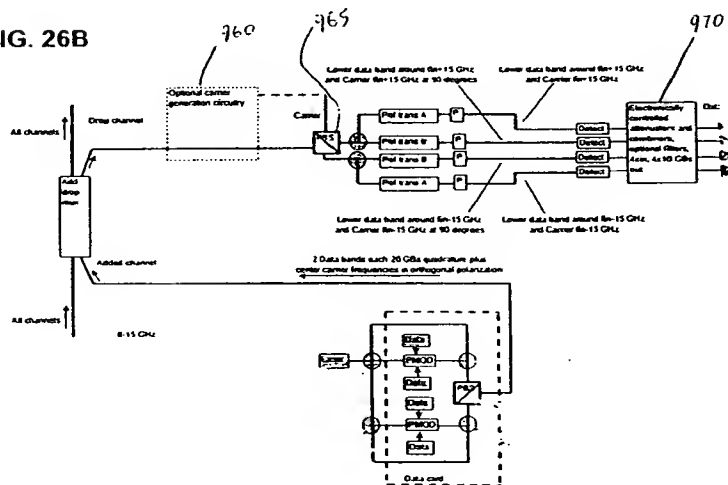


FIG. 26B



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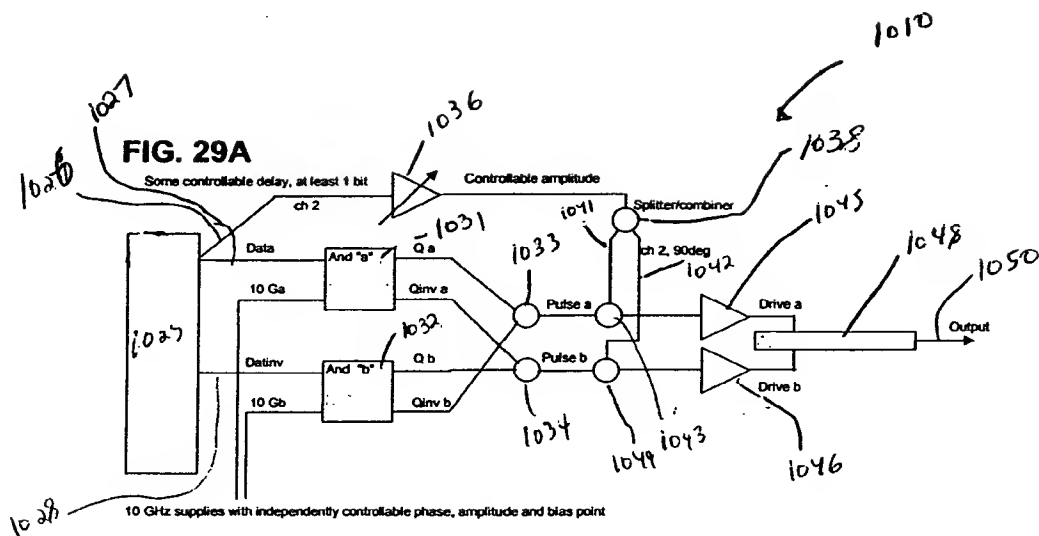
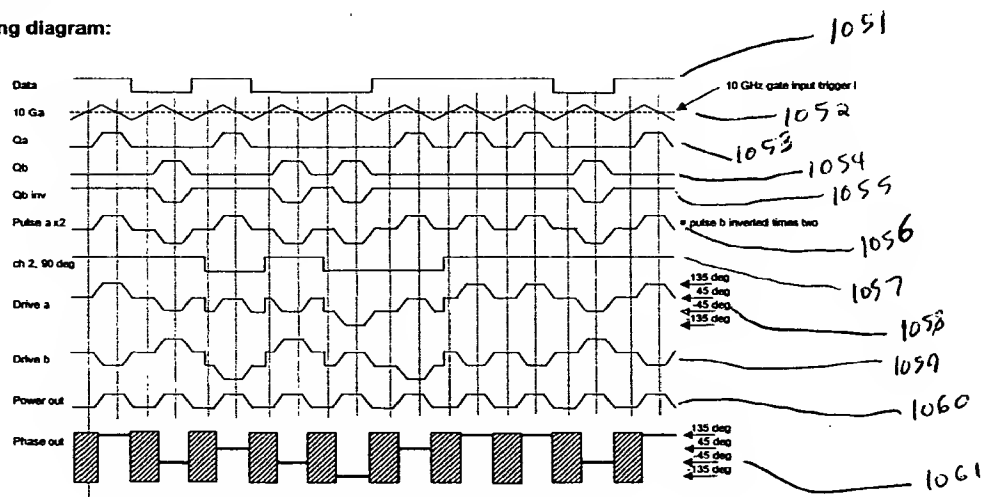
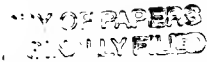


FIG. 29B

Timing diagram:





1100

